

1 18. The data communication system of Claim 12, wherein the reset circuit is a pre-
2 charge circuit.

1 19. The data communication system of Claim 12, wherein the reset
2 control signal is a pulse signal generated by a pulse generator.

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1 20. The data communication system as in Claim ¹²~~21~~, wherein the pulse generator is
2 triggered by a signal indicative of the input monitor signal.

1 21. A method for transferring data in a data communication system for a
2 semiconductor memory system having at least one data path comprising the steps of:
3 connecting a central data path to the at least one data path at a junction circuit;
4 receiving data in the junction circuit;
5 processing the data;
6 transferring the data out of the junction circuit;
7 resetting of the junction circuit for preparation for receipt of new data; and
8 controlling the resetting to prevent resetting while the data is being at least one
9 of received and processed.

1 22. The method of Claim 21, further including the steps of:
2 receiving an input monitor signal indicating that the data is being transferred
3 to the junction circuit; and